Docket No. TRANSMITTAL OF FORMAL DRAWINGS FIS920030199US1 Huagie Chen, et al. In Re Application Of: **Art Unit** Filing Date Confirmation No. Examiner Serial No. 8/4/03 10/604,607 STRUCTURE AND METHOD OF MAKING STRAINED SEMICONDUCTOR CMOS TRANSISTORS HAVING LATTICE-MISMATCHED SOURCE AND DRAIN REGIONS Invention Address to: Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450 Transmitted herewith are: 5 sheets of formal drawing(s) for this application. X Each sheet of drawing indicates the identifying indicia suggested in 37 CFR Section 1.84(c).

Howiel Shurua

H. DANIEL SCHNURMANN AGENT REGISTRATION NO.: 35,791 Dated: SEPTEMBER 23, 2003

I certify that this document and attached formal drawings are being deposited on September 23, 2003 with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature of Person Mailing Correspondence

Karen Cinq-Mars

Typed or Printed Name of Person Mailing Correspondence